Utilizing Circuit Simulator API to Perform Complex Custom Analysis in Advanced Process Node

Oracle / Silvaco

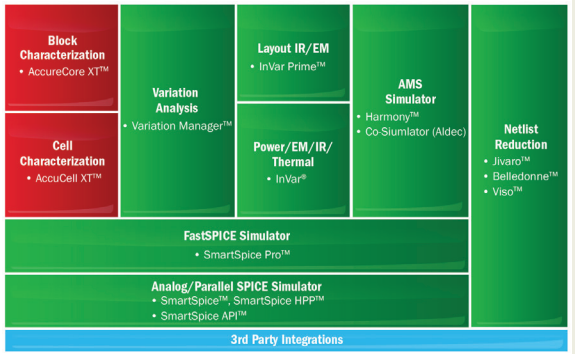
ABSTRACT

Circuit design in high-performance CPU requires complex simulation and analysis due to the need for high speed and high reliability. For critical circuits like high-speed SRAM, our methodology is to perform a full block level analysis on timing, power and signal integrity with detailed probing on every instance and net. The analysis results provide insight to designers to fine tune specific gate and transistors to maximize the performance of the circuits. To enable this methodology, the circuit is partitioned based on Channel Connection Region (CCR), then simulated and tracked in SPICE-level accuracy. We utilize SmartSpice API mode to speed up the simulation and track the results without file I/O; significantly improve analysis run-time and analyze the data in highly organized manner. The API mechanism is deployed in our CPU design in the FinFET process including 10nm and 7nm nodes; advanced modeling such as self-heat is also used. This presentation will introduce our analysis methodology using SmartSpice API and the benefits we have observed.

Silvaco EDA Provider

Silvaco is a leading EDA software and services provider founded in 1984.

- Strong Simulation Portfolio for design and verification
- **SmartSpice supports N7**
- Broad tool set delivering high accuracy and performance
  - Analog SPICE
  - FastSPICE
  - Variation Analysis
  - EM/IR/Thermal
  - RCLK Reduction



Agenda

Silvaco: SmartSpice API

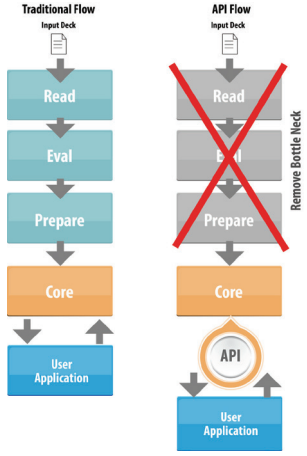
- Introduction & Overview
- SmartSpice advanced models technologies
- Silvaco SmartSpice API Technology
- SmartSpice API simulation flow under user application
- SmartSpice API functional integration
- SmartSpice API based Parallel Computing
- SmartSpice API: High Performance - SPICE Accurate
- Summary

Oracle: Transistor Power Analysis Methodology

- Overview of power analysis flow for SPARC processor cache memory
- Detail transistor level power analysis flow
- Advanced features for further analysis
- Results & Summary

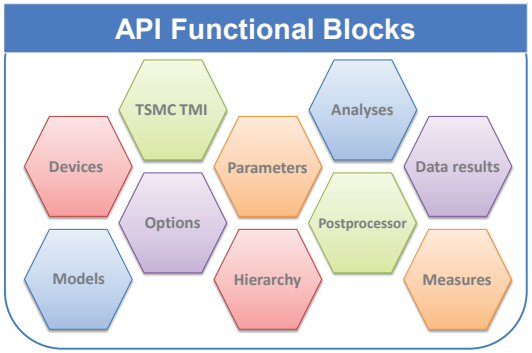
SmartSpice API Introduction

- User application uses SmartSpice library provided by Silvaco to get access to SmartSpice API (Application Programmable Interface)
- API is developed for high performance, accurate embedded application
- User application calls functions from SmartSpice API
- API contains around hundred functions to control simulator parser, simulation engine and postprocessor
- Silvaco provides C++ template as a starting point for user application integration

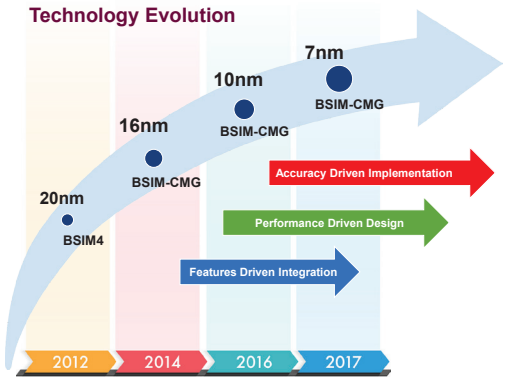


SmartSpice API Functionality Overview

- Functional control of .lib PVT corners
- Parametrization of PWL stimuli
- Extract nodes V/I
- Measure setup, hold and delays
- Set initial conditions
- Add and remove devices
- Control over synthesized SPICE objects



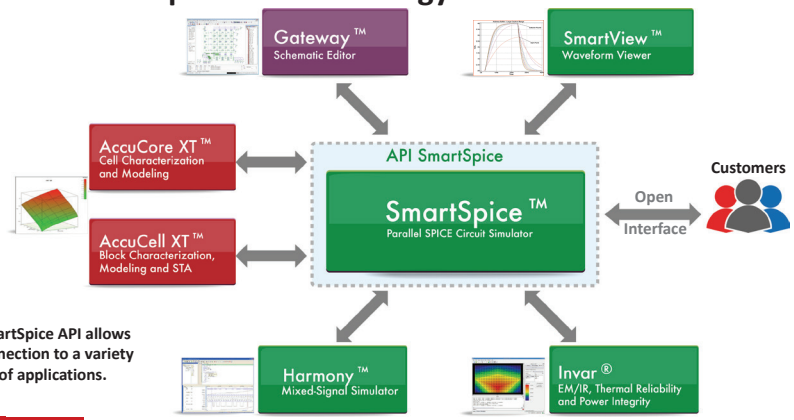
SmartSpice Advanced Models Technologies



Designer Features

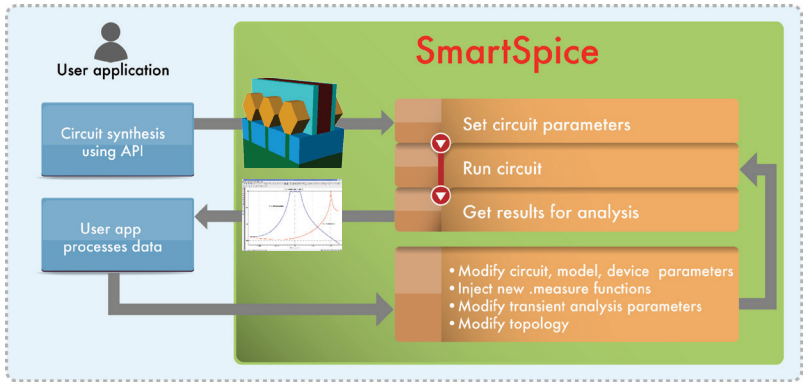
- Safe Operating Area (SOA) check
- Noise
- Monte Carlo simulation
- Aging analysis
- Self heating
- TSMC TMI model format compatibility

Silvaco SmartSpice API Technology

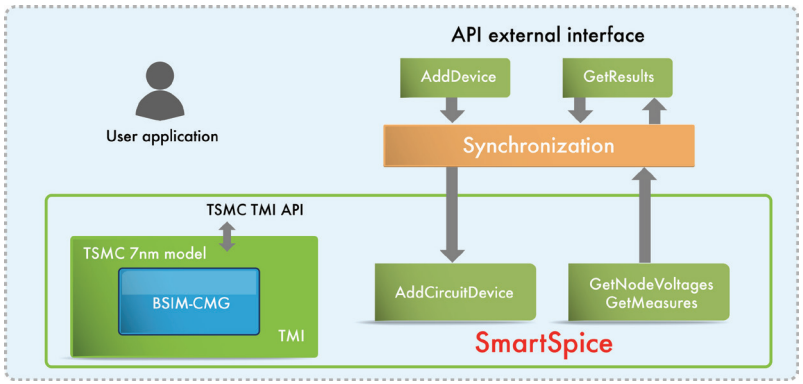


SmartSpice API allows connection to a variety of applications.

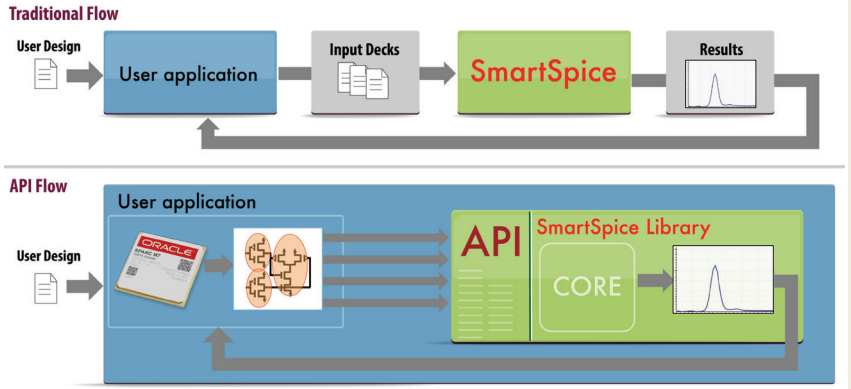
SmartSpice API Simulation Flow Under User Application



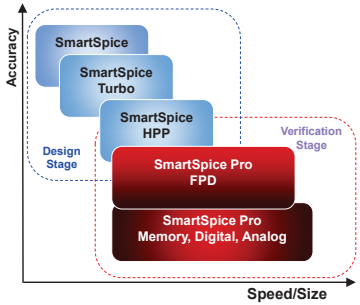
SmartSpice API Function Call Example



SmartSpice API based Parallel Computing



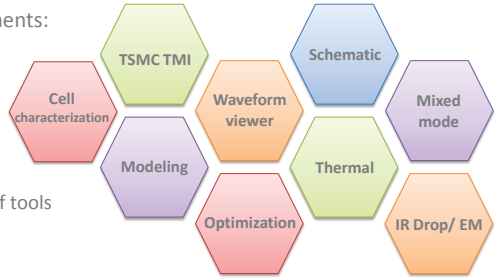
SmartSpice API: High Performance - SPICE Accurate



- Adoption of new technology nodes
- Improved designer productivity
- Strong and productive collaboration with Industry Leaders

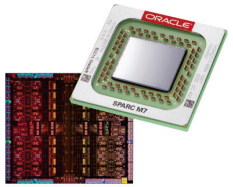
SmartSpice API Summary

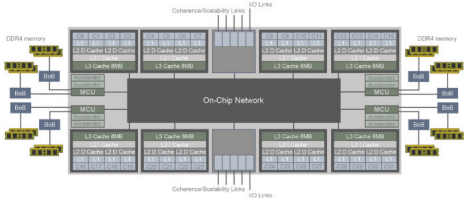
- Unique circuit simulation software technology
- Designed for high performance & accuracy driven applications
- Suitable for multiple industry segments:
  - Cell characterization
  - Schematic capture tools
  - Mixed mode applications
  - Waveform viewers
  - Modeling tools
  - Thermal/power/IR drop/EM signoff tools
  - Optimization tools



SPARC : High Performance CPU

- SPARC M7 Processor
  - SQL in silicon
  - Data Analytic Accelerators (DAX)
- Design Highlights
  - 32 cores, 8 threads per core
  - 4.13 GHz, 20nm





http://www.oracle.com/technetwork/server-storage/sun-sparc-enterprise/documentation/sparc-t7-m7-server-architecture-2702877.pdf

SPARC : High Speed SRAM Design

- 64MB L3 cache sub-system supports application data integrity
- 256KB L2 data cache for each core pair
- SRAMs are optimized for power-speed trade-offs
- Multiple Vt devices used extensively
- Stacked PMOS, Dummy Transistors, and NMOS standby-on used

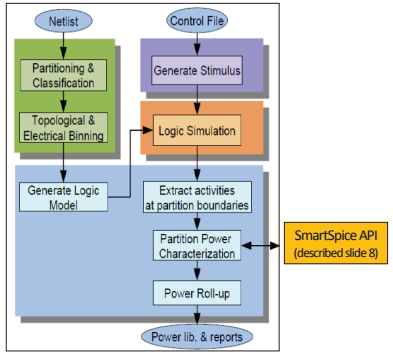
Reference:
M7: Oracle's Next-Generation Sparc Processor, IEEE Micro
P. Li, et al., 'A 20nm 32-core 64MB L3 cache SPARC M7 processor', 2015 ISSCC

Power Analysis in SPARC Processor SRAM

- SRAM contributes major portion of total power
- Power Analysis for SRAM needs to be accurate, fast and scalable
- Simulation with fully flat design for power analysis does not scale well with large number of cycles
- Accurate power rollup impossible with flat analysis
- Need to analyze power result in detail to improve/optimize SRAM designs
- Need fine-grained power data to find power hot-spots

SRAM Power Analysis Tool

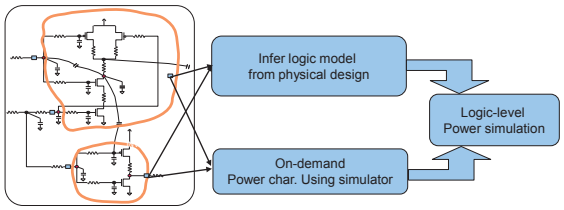
- SRAM power analysis tool has been used for over 5 years (20nm node and beyond)
- Fast, Accurate SRAM power analysis tool
  - Internally developed
  - Partitioning SRAM design using Channel Connected Region (CCR)
  - Create logic model and run logic simulation to get sensitization vectors
  - Build power models using spice simulator
  - Roll-up SRAM power numbers (cycle-by-cycle)



Reference:
Seokjoong Kim, Aravind Oommen, Krishnan Sundaresan, Haixin Liu and Jamil Mohd, *"Accurate Fast Power Analysis Methodology for SPARC Processor Cache Memory," Designer Track, 301.22, Design Automation Conference (DAC), Jun, 2014*

Partitioning & Logic Model Generation/Simulation

- Partitioning uses circuit classification, pattern match & representative analysis (RA)



Physical netlist (several thousand/million devices & several GB file size)

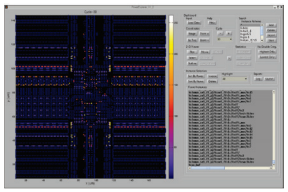
- Automated method to construct Verilog models from partitions
- Can handle complex partitions e.g., flops, latches, memory columns, etc.
- Employed Verilog simulation for fast logic sim.

Power Characterization of Partitions

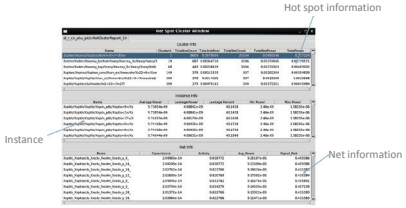
- Use SmartSpice API to characterize partitions on-the-fly
- Good accuracy correlation when comparing SPICE running on entire block
  - within 2% for voltages
  - within 5% for currents
- Faster and more scalable than other solutions

Advanced Features for Further Analysis

- More fine-grain power analysis : Cycle-by-cycle based, Hierarchical Instance based



<Layout-based SRAM power hotspot viewer>

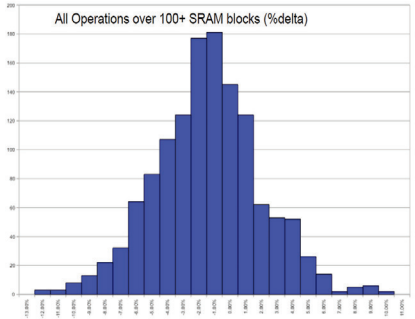


<SRAM power analytic platform>

- Advanced feature for accurate SRAM Power
  - SRAM power analysis using RTL power FSDB dump
  - Tool can run on huge activity dump (over 10K cycles) to report cycle-by-cycle power
  - Traditional SRAM power analysis tools were not able to do within reasonable time

Results

- Our SRAM power analysis tool was used on all SRAMs
- All operation's accuracy statistics
  - From all SRAMs (20nm node and beyond)
  - Each operations (such as RD, WR, CAM and LK
    - Avg. error rate = -0.56%
    - Std deviation = 3.48%



Summary

- Developed scalable power analysis solution for high-speed SRAM design
- Can handle large number of cycles (over 10K), and RTL FSDB dump as stimulus to see power numbers in cycle-based manner
- Built-in power profiling / Fine grained power debugging
- Integrated solution with other flows such as analyzing power hot-spot in large SRAM design

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Hardware and Software
Engineered to Work Together

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